

**WHAT IS CLAIMED IS:**

1 1. A semiconductor device comprising:  
2 a semiconductor substrate in which a source, drain and channel are  
3 formed;  
4 a gate formed on a gate dielectric layer formed on the semiconductor  
5 substrate;  
6 spacers adjacent to the gate wherein the gate and spacers are formed  
7 in a trench formed in a layer of dielectric material formed on the substrate  
8 surface.

1 2. The semiconductor device of claim 1 wherein the distance between  
2 the spacers defines a device gate length.

1 3. The semiconductor device of claim 2 wherein the distance between  
2 the spacers is less than 50 nm.

1 4. A process for device fabrication comprising:  
2 forming a sacrificial gate over an active region of a semiconductor  
3 substrate wherein the width of the sacrificial gate is selected to define the  
4 distance between a source region and a drain region in the semiconductor  
5 substrate;  
6 forming a trench dielectric layer adjacent to the sacrificial gate;  
7 removing the sacrificial gate, thereby defining a trench in the trench  
8 dielectric layer;  
9 forming spacers in the trench; and  
10 forming a device gate in which at least a portion of the gate is formed  
11 between the spacers.

1           5. The process of claim 4 wherein a first layer of dielectric material is  
2 formed on the semiconductor substrate before the sacrificial gate is formed  
3 thereon and wherein the sacrificial gate is formed on the active region of the  
4 substrate.

1           6. The process of claim 5 wherein the active region in the  
2 semiconductor substrate is defined by shallow trench isolation.

1           7. The process of claim 6 further comprising implanting dopant into  
2 the semiconductor substrate after the sacrificial gate is formed thereover,  
3 wherein the implant conditions are selected to define a source and a drain  
4 region in the semiconductor substrate.

1           8. The process of claim 6 further comprising implanting dopant into  
2 the semiconductor substrate after the spacers are formed thereover.

1           9. The process of claim 6 wherein the gate is formed by:  
2 forming a gate dielectric layer between the spacers;  
3 forming a gate electrode over the gate dielectric layer;  
4 forming a layer of metal over the gate electrode; and  
5 patterning the layer of dielectric material with the layer of metal  
6 thereover to form the gate.

1           10. The process of claim 4 wherein the trench dielectric layer is  
2 formed by:  
3 depositing a layer of trench dielectric material over the substrate with  
4 the sacrificial gate thereon;  
5 polishing the layer of trench dielectric material; and  
6 stopping the polishing of the trench dielectric material after the  
7 sacrificial gate is exposed therethrough.

1 11. The process of claim 10 wherein the trench dielectric layer is a  
2 layer of silicon dioxide and the sacrificial gate is silicon nitride.

1 12. The process of claim 11 wherein the trench dielectric layer is  
2 deposited from a high density plasma.

1 13. The process of claim 11 wherein the sacrificial gate is removed  
2 using a wet etch.

1 14. The process of claim 11 wherein the spacers are silicon nitride.

1 15. The process of claim 11 wherein the spacers are formed by:  
2 depositing a layer of silicon nitride on the surface of the semiconductor  
3 substrate with the trench dielectric layer thereon after the trench is formed  
4 in the trench dielectric layer; and  
5 anisotropically etching the silicon nitride layer to form the spacers.

1 16. The process of claim 15 further comprising a local channel implant  
2 after the spacers are formed.

1 17. The process of claim 15 further comprising a local channel implant  
2 after the trench is formed.

1 18. The process of claim 15 further comprising removing the oxide  
2 from a portion of the semiconductor substrate surface between the spacers.

1 19. The process of claim 9 wherein the gate dielectric layer is selected  
2 from the group consisting of silicon dioxide, silicon oxynitride and tantalum  
3 oxide.

- 1 20. The process of claim 9 wherein the gate electrode is doped
- 2 polycrystalline silicon.

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